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Substitute for form 1449A ~~1449A~~

## **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

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Sheet 1 of 2

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>			
(Use as many sheets as necessary)			
Sheet	1	of	2
		Application Number	10/672,895
		Filing Date	September 26, 2003
		First Named Inventor	Mira Ben-Tzur
		Art Unit	not yet known 2813
		Examiner Name	not yet known NGUYEN
		Attorney Docket Number	10002.000810 (PM02006-2)

## U.S. PATENT DOCUMENTS

## FOREIGN PATENT DOCUMENTS

Examiner Signature	T. NGUYEN	Date Considered	5/2/04
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INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

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Sheet 2 of 2

## Complete If Known

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Filing Date	September 26, 2003
First Named Inventor	Mira Ben-Tzur
Art Unit	not yet known 2813
Examiner Name	not yet known NGUYEN

Attorney Docket Number 10002.0000810 (PM02006-2)

## NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
TN	G	SEONG GEON PARK, et al. "A New ALD-TiN/CoSi2 Contact Plug Process for Reliable and Low Defect Density Bit-Line Integration in Sub-Quarter Micron Giga-bit DRAM" IEEE 2002, pgs. 282-284; Semiconductor R&D Center, Samsung Electronics Co, LTD., KOREA.	
TN	H	J.T. WETZEL, et al. "Evaluation of Material Property Requirements and Performance of Ultra-Low Dielectric Constant Insulators for Inlaid Copper Metallization" IEEE 2001, pgs. 4.1.1 - 4.1.3; Int'l Sematech, Austin, TX; Texas Instruments, Dallas, TX; Motorola, Austin, TX; TSMC, Taiwan; IBM, Burlington.	
TN	I	M. BEN-TZUR, et al. "Integrated of Low-K Dielectrics in The Passivation Level of Al-Based Multilevel Interconnect Technology" submitted for Publication March 2002, (2 pgs); Cypress Semiconductor, San Jose, CA., USA.	
TN	J	WEI-JEN HSIA, et al. "Flowfill Technology Low Dielectric Constant Materials" Retrieved from the internet:<URL: http://www.trikon.com [printed on 3/29/02] (4 pgs); LSI Logic, CA; Trikon Technologies Ltd.	
TN	K	BRUCE W. McGAUGHEY, et al. "A Simple Method for On-Chip, Sub-Femto Farad Interconnect Capacitance Measurement" IEEE Vol. 18, No. 1 January 1997, pgs. 21 - 23; University of California, Berkeley, CA., USA	
TN	L	Conference highlights latest data on SILK resin, expanded Alliance membership, (3 pgs); December 5, 2001; The Dow Chemical Company and Loomis Group; Midland, Michigan, USA.	
TN	M	INTERCONNECT; The International Technology Roadmap For Semiconductors, pgs. 1 -25, 2001 Edition.	

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